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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,664	03/17/2004	Shawn D. Rogers	13050/12	2665

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,664	ROGERS ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) *8-47,49-51,55-57 and 61-71* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,48,52-54,58-60 and 72* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/13/2007 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-4, 7, 48, 52-54, 58-60, and 72 are rejected under 35 U.S.C. § 102(b) as being anticipated by HERNANDEZ (RE35,064).

With regard to claims 1-4, 7, and 72 Hernandez discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 132; a second conductive layer 98 (the second conductive layer is visible, but not numbered, in figure 13. It is the conductive layer separated from lattice 124 by a first dielectric layer 92, also not numbered in figure 13 but numbered 12 (figure 9 shows numeral 12, but that part is referred to in figure 10 and the written description as dielectric layer 92. The written description does not refer to a part #12 in figure 9) in figure 9. Since figure 9 uses part #98 to refer to the second conductive layer, and figure 13 uses no part #, the second conductive layer will be referred to, for convenience, as part #98) separated from first conductive layer 132; first conductive rods 120 (not numbered in figure 13, the same part is numbered 120 in figure 12) comprising plated vias passing through a first dielectric layer 92 (see the discussion above concerning second conductive layer 98. The first dielectric layer is shown without reference # in figure 13, referenced as part #12 in figure 9, and discussed in the written description as part #92) disposed between the first 132 and second 98 conductive layers, connected to the second conductive layer 98, and extending to the first conductive layer 132; and chip capacitors 102, each having a same capacitance value, arrayed over substantially an entire area of the first conductive layer 132, connecting the first conductive rods 120 to the first conductive layer 132, and arranged in a lattice 124. Note figures 7-10 and 13 (note that figure 13 employs two lattices 124 and 126 of the sort shown in detail in figure 9 as lattice 96, said lattice 96 be-

ing identified as a lattice 44 of chip capacitors 102 in figures 6-8, the construction of said lattice 44 being detailed in figures 6-8.The rectangular lattice of chips 102 is best seen in cutaway figure 10), column 5 lines 19-36, column 6 lines 2-24 and 65-67, and column 7 lines 1-8 of Hernandez. Note that at column 5 lines 20-22, Hernandez specifically states that the lattice-arrayed spaced ceramic chip 102 of figures 9-12 may be either a high dielectric constant pellet of homogeneous composition (described at column 1 lines 62-67 and shown in figures 1-4) or a multilayer capacitive element (a known multilayer ceramic chip) capacitor 44, as described at column 5 lines 20-40.

With regard to claims 48, 52-54,58,59, and 60 Hernandez discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 132 of a multilayered printed circuit board; a second conductive layer 98 (the second conductive layer is visible, but not numbered, in figure 12. It is the conductive layer separated from lattice 124 by a first dielectric layer 92, also not numbered in figure 13 but numbered 12 (figure 9 shows numeral 12, but that part is referred to in figure 10 and the written description as dielectric layer 92. The written description does not refer to a part #12 in figure 9) in figure 9. Since figure 9 uses part #98 to refer to the second conductive layer, and figure 12 uses no part #, the second conductive layer will be referred to, for convenience, as part #98) of said multilayered printed circuit board separated from the first conductive layer 132; a plurality of conductive rod pairs 118-120 disposed in a rectangular periodic pattern; and a first capacitor 102 disposed on an outer surface of the printed

circuit board and connecting a proximate end of a first conductive rod 120 and a second conductive rod 118; said first conductive rod 120 being connected to the first conductive layer 132 and traversing the second conductive layer 98; said second conductive rod 118 being connected to the second conductive layer 98 and traversing the first conductive layer 132, wherein the first conductive rod 120 and the second conductive rod 118 are disposed adjacent to each other and form one of said plurality of conductive rod pairs 118-120. Note figures 7-10 and 12 (note that figure 12 employs lattice 96 as shown in detail in figure 9, said lattice 96 being identified as a lattice 44 of capacitors 102 in figures 6-8, the construction of said lattice 44 being detailed in figures 6-8.The rectangular lattice of chips 102 is best seen in cutaway figure 10), column 5 lines 19-36, column 6 lines 2-24 and 65-67, and column 7 lines 1-8 of Hernandez.

The applicant's claims 59 and 60 do not distinguish over the Hernandez reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of accommodating circuit components and accommodating signal and ground connections.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. See *In re Ludtke and Sloan*, 169 USPQ 563 at 567, and *In re Swinehart* 169 USPQ 226, both of which make it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or

obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also In re Schreiber, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997), for a discussion of the roles of examiner and applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

B. Claims 48, 52-54, and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by MCKINZIE III (6,476,771).

With regard to claims 48, 52-54, and 58, McKinzie III discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 903 of a multilayered printed circuit board 900; a second conductive layer 901 of said multilayered printed circuit board 900 separated from the first conductive layer 903; a plurality of conductive rod pairs 921-922 disposed in a rectangular periodic pattern (see fig. 9B); and a first capacitor 911 (McKinzie III refers to the capacitors 911 and 914 as a "capacitive frequency selective surface (FSS)") disposed on an outer surface of the printed circuit board 900 and connecting a proximate end of a first conductive rod 922 and a second conductive rod 921; said first conductive rod 922 being connected to the first conductive layer 903 and traversing the second conductive layer 901; said second conductive rod 921 being connected to the second conductive layer 901 and traversing the first conductive layer 903, wherein the first conductive rod 922 and the second conduc-

tive rod 921 are disposed adjacent to each other and form one of said plurality of conductive rod pairs. Note figures 9A-9B and column 5 lines 10-67 of McKinzie III.

Allowable Subject Matter

3. Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 12/13/2007 have been fully considered but they are not persuasive.

It is argued, at page 15 of the remarks, that "The Applicants respectfully submit that the actual requirement is somewhat more restrictive."The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." (*In re Cortright,* 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)). MPEP 2111, second paragraph (emphasis added)."

The *Cortright* court held that, consistent with its appellant's disclosure and the disclosure of three patents from analogous arts using the same phrase to require only some increase in hair growth, one of ordinary skill would construe "restore hair growth" to mean that the claimed method increases the amount of hair grown on the scalp, but does not necessarily produce a full head of hair. See MPEP § 2111, ¶ 2. The present

situation distinguishes from *Cortright* in that any and all definitions of "chip capacitor" are consistent with Applicant's disclosure. Applicant's disclosure does not state any properties[1] a "chip capacitor" may or may not have. nor does Applicant's disclosure does state that a "chip capacitor" may have any particular structure. As for "three patents from analogous arts using the same phrase," the Examiner suggests Applicant consult U.S. Pat. Nos. 4,745,537 and 4,706,162, and Reissue No. RE35064, all of which use "chip capacitor" (the "same phrase") in a manner consistent with the multilayer capacitive element 44 of the Hernandez disclosure. Note, for example, column 5 line 23 of Reissue No. RE35064. This is perhaps not a surprising result, because RE35064 (one of "three patents from analogous arts using the same phrase") is the Hernandez disclosure, and RE35064 refers its readers to U.S. Pat. Nos. 4,745,537 and 4,706,162 for a full definition of "chip capacitor." If *Cortright* had been based on facts in analogous to the present facts, the *Cortright* appellant's disclosure would not have said a word about how much hair was grown in the process of "restor[ing] hair growth" while the "three patents from analogous arts" would have used the same phrase to mean "producing a full head of hair."

At page 15 Applicant further argues that "Hernandez teaches a 'high capacitance flexible dielectric sheet' or 'high dielectric flexible sheet' (Hernandez, col. 2 lines 24-32).

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[1] Applicant's disclosure does not state a single word about what a "chip capacitor" is or how it works. Not a word about how big a "chip capacitor" is. Not a word about what materials a "chip capacitor" is formed

This sheet is 'comprised of a monolayer of multilayer or single layer high dielectric constant (e.g., ceramic) s or pellets ... arranged in a planar array.' (Id., col. 1, lines 62-67.) The dielectric material has a typical dielectric constant of 15,000 (Id., col. 4, line 55). '[T]he dielectric sheet is electroless plated with copper or nickel.'" However, Applicant's argument ignores the fact that Hernandez also teaches, "Still another embodiment of the present invention is shown in FIGS. 6-8. In this embodiment, rather than using high dielectric constant pellets of homogeneous composition, a multilayer capacitive element 44 is utilized. Capacitive element 44 is a known multilayer ceramic chip capacitor" (emphasis added). Note column 5 lines 19-24 of Hernandez. When arguing a given set of facts, Applicant is urged to consider all the facts in said set of facts.

It is argued, at page 16 of the remarks, that "It is evident from the description that the metallization extends over a plurality of dielectric s in a contiguous area, and that therefore each element 102 of the reference is a single ceramic chip, and not a capacitor. The Applicants respectfully submit that element 102 is a chip of dielectric material, and not a chip capacitor." Applicant's conclusion, although persuasive on its face, does not account for the fact that Hernandez teaches an alternate embodiment in which a "multilayer chip capacitor" (note that these are Hernandez's exact words) is substituted for said "chip of dielectric material."

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from. Not a word about the structure a "chip capacitor" should have. Applicant's disclosure does not even state how much hair a "chip capacitor" restores

On page 16 Applicant further argues that "In the advisory action, the Examiner asserts that the term "capacitors' (which term must necessarily encompass any and all electrical elements capable of capacitive functioning) .... ' (Advisory action, page 4). The Examiner has not, at least in the advisory action, identified the specific structure that would meet the definition used by the Examiner, and the Applicants respectfully request that the Examiner make reference to a specific structure." It has already been explained to Applicant (several times) that McKinzie III refers to the claimed capacitor as a "capacitive frequency selective surface (FSS)." See, for example, page 6 lines 12-13 of the final rejection mailed 6/18/07. However, in response to Applicants' current request that the Examiner make reference to a specific structure in McKenzie III that meets the definition of "electrical elements capable of capacitive functioning," the Examiner will state for the record that in McKenzie III the "capacitive frequency selective surface (FSS)" is an electrical element capable of capacitive functioning. Note that McKenzie III discloses many such structures, in fact a whole array of such structures.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826